IR Enhanced Global Shutter Pixel for High Speed Applications

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***Abstract* -This paper presents the methods used to enhance the near IR performance of a 3.75µm global shutter pixel. We will show that we could achieve Quantum Efficiency (QE) above 30% at 850nm while keeping the Modulation Trasfer Funcition (MTF) in our test system above 40 lpm (at 50%). We will present the tradeoff we found between the Quantum Efficiency and the MTF while using different epi thickness and resistivity. The pixel is targeted for different markets including automotive and security and was tested on silicon for up to 450 fps.**

***Keywords*—Near Infra Red, CIS, Global Shutter, High Frame Rate, MTF**

I. INTRODUCTION

In recent years there is a strong market demand for global shutter CMOS Image Sensors[1,2]. One emerging application for this technology is for sensors in human recognition systems for consumer, automotive and security applications. Such systems are highly portable, which pushes global shutter pixel pitch below 4µm. Such systems are typically working in the near IR regime, at the range of 820 to 850nm, which dictate special optimization of the pixel structure in order to reach high quantum efficiency and at the same time minimizing the pixel cross-talk.

A VGA test chip working at speed up to 450fps is presented. The chip was built in IS11 process node from TJ [3]. We used a 5T pixel. The Pixel pitch is 3.75µm and the Memory Node (MN) structure was optimized for low dark current and low parasitic IR light sensitivity using special implants as reported by Lahav at al [4]. The sensor includes internal charge pump which allows boosting of the pixel reset signal up to 0.5V above its VDD.

II. PIXEL CONCEPT AND INTEGRATION

One of the main challenges for IR enhanced application is the pixel optimization for both high QE and low x-talk in the near IR regime. The optimization approach we have chosen was a combination of relatively deep diode implant [6] and fabrication on a High Resistivity (HR) epi starting material. The CMOS digital and analog parts of the chip are implanted with deep P-Well (DPW) which is designed to maintain: a) N-Well to N-Well isolation with the same space as in the original technology; b) keep CMOS parameters without significant change in compare to standard wafer. This saved the need for re-characterization and modeling of the basic transistors of the technology.

For starting material with 1000 Ω-cm, the pinned diode maximum potential was set to 1.5V and the depletion region penetrates about 10.5μm into the silicon. The potential contour map for a simplified cut across the pixel array is shown in Figure 1. It is shown that a single diode is electrically isolated from its adjacent diode up to 2.5um from the silicon surface. Deeper than that the diodes potential superimpose and virtually creates straight equipotential lines. Simulation of a steady state electron concentration under 850nm illumination in the center of one diode is shown in Figure 2. The case of 12μm epi with 1000Ω·cm is shown in Figure 2(a) and the case of TowerJazz (TJ) standard 30Ω·cm 12μm epi Ω-cm is shown in Figure 2(b). It is clear that in the HR case the generated electrons are drifted towards the silicon surface perpendicular to the straight equipotential lines. When they reach ~2.5μm from the surface the equipotential bends the current towards the illuminated diode. As expected, in the Low Resistivity (LR) case the electrons are laterally diffused and less electrons are collected by the illuminated diode, The rest of the electrons reach adjacent diodes, and cause degradation of MTF.

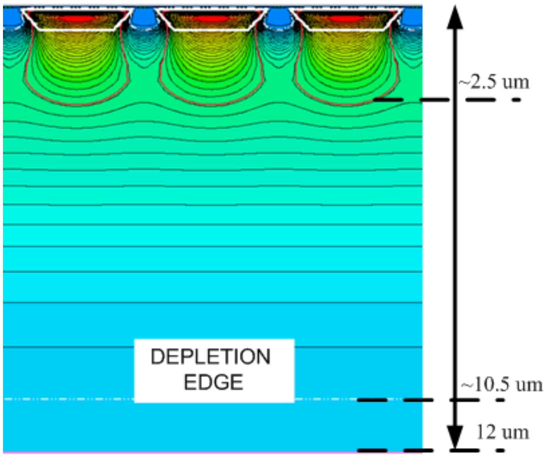

Figure 1. Simulated potential profile for 12um HR wafer. The 2D cut is performed across the pixel array. Pixel pitch is 3.75μm.

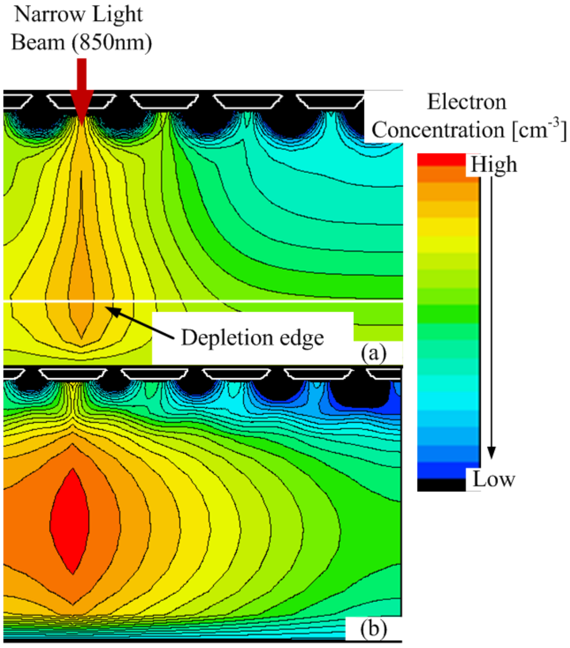

Figure 2.Simulated Electron concentration is steady state. (a) – HR case (b). LR case. light is impinging in narrow column centered on the first diode. Simulated wavelength is 850 nm

Another interesting feature should be emphasized in the case of HR. The charge column widens under the edge of depletion region due to diffusion. This mechanism degrades the MTF when the thickness of starting material is not tailored to the depletion region edge.

III. RESULTS

The VGA test chip was manufactured using high resistivity starting materials with different thicknesses. As a reference we manufactured the sensor on a 5.5µm and 12µm epi with standard resistivity. The QE was measured with a narrow band filter centered at 850nm. The MTF was measured with the same narrow band filter and a module lens. The module lens limits the MTF and the measurement in the standard resistivity 5.5µm epi can be considered as the upper limit for the measured MTF. The results are summarized in Figure 3. The MTF of the sensor manufactured on 12µm HR is 30% higher than the MTF measured on the sensor manufactured on 12µm LR. As estimated before below 10µm, the HR sensor can be considered as a fully-depleted one and shows MTF very close to the upper limit of the module. The QE follows the starting material thickness as expected. The main parameters of the pixel are summarized in Table1.

IV. SUMMARY

In this paper we report the optimization performed on a 3.75µm pixel embedded in an IR Enhanced global Shutter sensor test chip for high speed application. We have shown that by choosing high resistivity material with appropriate thickness we can optimize both MTF and QE.

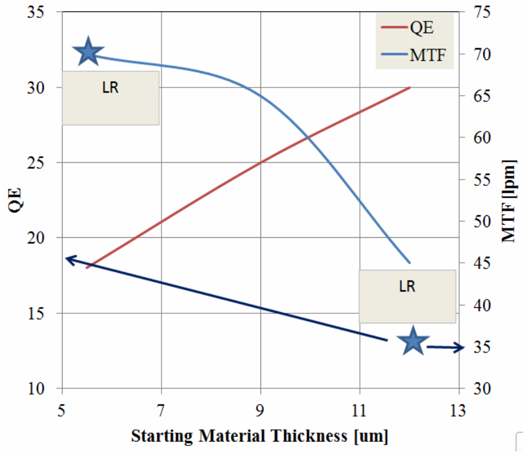

Figure 3 Experimental result for QE and MTF measured at 850nm on the VGA sensor. The MTF was measured with module filter and module lens using IMATEST software and test charts [7]

Parameter	Unit	Value
Pixel Pitch	**um**	**3.75**
Temporal Noise	**mV**	**~1.5**
PRNU [525nm]	**%**	**0.6**
CG	**uV/e**	**100**
Saturation Well	**e**	**20k**
QE [525nm]	**%**	**50**
PLS [525nm]		**<1000**

Table 1. Performance summary

V. REFERENCES

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